pattern formed on a substrate; an inter-layer insulating film which covers said conductive layer pattern and is formed on said substrate; a first connection hole formed in a upper layer of said inter-layer insulating film above said conductive layer pattern; a second connection hole which reaches said conductive layer pattern from the bottom portion of said first connection hole and then has a smaller diameter than that of said first connection hole and formed on said inter-layer insulation film; a plug having conductivity formed in a state filling internal portions of said first connection hole and said second connection hole; an upper insulating film formed on said inter-layer insulating film; a third connection hole which reaches said plug and is formed on said inter-layer insulating film; and a conductive portion which is connected to said plug and formed in said third connection hole.

Independent claim 4 recites--a semiconductor device, comprising: a conductive layer pattern formed on a substrate; an inter-layer insulating film which covers said conductive layer pattern and is formed on said substrate; a first connection hole formed in a upper layer of said inter-layer insulating film above said conductive layer pattern; a second connection hole which reaches said conductive layer pattern from the bottom portion of said first connection hole and then has a smaller diameter than that of said first connection hole and formed on said inter-layer insulation film; a plug having conductivity formed in a state filling internal portions of said first connection hole and said second connection hole, wherein the upper surface of said plug is formed to almost the same height as the surface height of said inter-layer insulating film; an upper insulating film formed on said inter-layer insulating film; a third connection hole which reaches said plug and is formed on said inter-layer insulating film; and a conductive contact portion which is connected to said plug and formed in said third connection hole.

Figs. 1-17 and corresponding portions of the specification disclose methods of manufacturing a so-called capacitor-over-bit-line type dynamic random access memory. In a first

method, a diffusion layer 12 is formed on a substrate 10. An inter-layer insulating film 21 is then formed formed on diffusion layer 12. A doped polysilicon film 31 is deposited on insulating film 21, and an aperture 32 is formed on doped polysilicon film 31. A side wall 33 is formed on aperture 32 and a first connection hole 22 is formed in insulating film 21 using the doped polysilicon film 31, and side wall 33 as a mask. A conductive layer 24 is formed on insulating film 21 so that conductive layer 24 covers first connection hole 22. Insulating film 21 then becomes lower layer insulating film 21. An upper layer insulating film 25 is formed on lower layer insulating film 21. Then a second connection hole 26 is formed in upper layer insulating film 25. A storage node contact 28 is formed by a conductive portion 27 located inside second connection hole 26. Conductive portion 27 on upper layer insulating film 25 forms part of the storage node 29.

In a second manufacturing method, *AAPA* discloses in Figs. 4-17 that various structures are formed on a silicon substrate PSUB through a number of oxidizing and etching steps. These structures include a number of bit line contact holes BCH and node contact holes NCH formed from apertures in substrate PSUB. See, for example, Fig. 8 and the specification at page 5, line 26 – page 6, line 5.

Indeed, in conventional methods, bit line contact holes and node contact holes are formed on a substrate. As shown in Fig. 8, however, the contact holes BCH and NCH are formed on substrate PSUB in a side-by-side manner. As a result, a second connection hole BCH does not reach said conductive layer pattern from the bottom portion of said first connection hole NCH, as recited in the claim. On the other hand, Fig. 1(3) shows that two connection holes 22 and 26 may be formed such that a first connection hole 22 may reach a conductive layer 24 from the bottom portion of a second connection hole 27, and that both connection holes are of the same diameter. The prior art does not disclose, teach, or suggest that either of the first or second

connection hole has a smaller diameter than the other connection hole.

In contrast, the claimed invention includes, a second connection reaches a conductive layer pattern from the bottom portion of a first connection hole and has a smaller diameter than that of said first connection hole and formed on said interlayer insulation film.

In sum, the prior art fails to disclose, teach, or suggest, every element recited in claim 3. Specifically, *AAPA* does not disclose, teach, or suggest, at least "a second connection reaches a conductive layer pattern from the bottom portion of a first connection hole and has a smaller diameter than that of said first connection hole and formed on said interlayer insulation film," as recited in the claim. To properly anticipate a claim, the document must disclose, explicitly or implicitly, each and every feature recited in the claim. *See* Verdegall Bros. v. Union Oil Co. of Calif., 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Because the prior art fails to disclose, either explicitly or implicitly, at least the above noted feature recited in independent claims 3, claim 3 is not anticipated. For at least this reason, Applicant submits that claim 3 is allowable and withdrawal of the §102 rejection is requested.

Based on the foregoing discussion, Applicant further submits that prior art also does not anticipate the subject matter recited in independent claim 4. Claim 4 recites, among other things, "a second connection hole which reaches said conductive layer pattern from the bottom portion of said first connection hole and then has a smaller diameter than that of said first connection hole and formed on said inter-layer insulation film." Thus, for at least the same reasons given above, Applicant respectfully requests the withdrawal of the §102 rejection of claim 4, and allowance of this claim.

Claims 5 and 6 depend from independent claims 3 and 4 respectively. By virtue of this dependency, Applicant submits that claims 5 and 6 are allowable for at least the same reasons

discussed above. Applicant respectfully requests that the rejection of claims 5 and 6 under §102 be withdrawn, and claims 5 and 6 allowed.

Conclusion

Based on at least the foregoing remarks, Applicant submits that claims 3-6 are allowable, and this application is in condition for allowance. Accordingly, Applicant requests favorable reexamination and reconsideration of the application. In the event the Examiner has any comments or suggestions for placing the application in even better form, Applicant requests that the Examiner contact the undersigned attorney at the number listed below.

Dated: February 5, 2003

Respectfully submitted,

By_____
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In the event additional fees are necessary in connection with the filing of this paper, or if a petition for extension of time is required for timely acceptance of same, the Commissioner is hereby authorized to charge Deposit Account No. 180013 for any such fees; and applicants hereby petition for any needed extension of time.

Appendix to Amendment--Version With Markings to Show Changes Made

3. (Twice Amended) A semiconductor device, comprising:

a conductive layer pattern formed on a substrate;

an inter-layer insulating film which covers said conductive layer pattern and is formed on said substrate;

a first connection hole formed in a upper layer of said inter-layer insulating film above said conductive layer pattern;

a second connection hole which reaches said conductive layer pattern from the bottom portion of said first connection hole and then has a smaller diameter than that of said first connection hole and formed on said inter-layer insulation film; [and]

a plug having conductivity formed in a state filling internal portions of said first connection hole and said second connection hole;

an upper insulating film formed on said inter-layer insulating film;

a third connection hole which reaches said plug and is formed on said inter-layer insulating film; and

a conductive portion which is connected to said plug and formed in said third connection hole.

4. (Twice Amended) A semiconductor device, comprising:

a conductive layer pattern formed on a substrate;

an inter-layer insulating film which covers said conductive layer pattern and is formed on said substrate;

a first connection hole formed in a upper layer of said inter-layer insulating film above said conductive layer pattern;

a second connection hole which reaches said conductive layer pattern from the bottom

portion of said first connection hole and then has a smaller diameter than that of said first connection hole and formed on said inter-layer insulation film; [and]

a plug having conductivity formed in a state filling internal portions of said first connection hole and said second connection hole[;] ,

wherein the upper surface of said plug is formed to almost the same height as the surface height of said inter-layer insulating film;

an upper insulating film formed on said inter-layer insulating film;

a third connection hole which reaches said plug and is formed on said inter-layer insulating film; and

a conductive contact portion which is connected to said plug and formed in said third connection hole.